



## INSTALLATION INSTRUCTIONS

1. Remove the cover plate from the appropriate option slot in the TSU/TDU/ESU rear panel.
2. Slide the Dual Nx 56/64 Module into the option slot until the module is firmly positioned against the front of the chassis.
3. Secure the thumbscrews at both edges of the module. Tighten with a screwdriver.
4. Connect the cables to the associated device(s).

## SPECIFICATIONS

<b>DTE Interface</b>	CCITT V.35 Synchronous
<b>Rates</b>	1.536 Mbps (T1) & 2048 Mbps (E1) in 56K or 64K steps
<b>Tests</b>	Local Loopback (Bilateral) - menu activated Remote Loopback (V.54) - menu activated Self-Test
<b>Test Pattern</b>	511 with errored seconds display and error inject capability
<b>1s Density Protection</b>	Forces 1s to network after one second of consecutive zeros from DTE
<b>Connector</b>	26-Pin Subminiature D

## 26-PIN SUBMINIATURE D PINOUT

Pin	Description
1	Frame ground (FG)
4	Request to send (RTS) from DTE
5	Clear to send (CTS) to DTE
6	Data set ready (DSR) to DTE
7	Signal ground (SG)
8	Received line signal detector (DCD) to DTE
9	Transmitted data (TD-A) to DTE
10	Transmitted data (TD-B) to DTE
11	Received data (RD-A) to DTE
12	Received data (RD-B) to DTE
13	External TX clock (ETC-A) from DTE
19	Test mode (TM) to DTE
22	TX clock (TC-A) to DTE
23	TX clock (TC-B) to DTE
24	RX clock (RC-A) to DTE
25	RX clock (RC-B) to DTE
26	External TX clock (ETC-B) from DTE

**MENU TREE**

Dual Nx56/64Menu	1) Status		1) DTE Data Clock
	2) Port Status		2) DTE Status
			3) Port Rate
	2) Config		1) Interface
	7) Port Config		2) Rate
			3) Tx Clk Cntrl
			4) Data
			5) CTS
			6) DCD
			7) DSR
			8) "0" INHIB
			9) Inband
			A) Tx Clk Source
	3) Util	6) Port Utility	SW Rev
	4) Test		1) Loopback
3) Port Test		2) 511 Patt	
		3) Disp 511 Rslt	

**V.35 WINCHESTER CONNECTION PINOUT**

Pin	CCITT	Description
A	101	Protective ground (PG)
B	102	Signal ground (SG)
C	105	Request to send (RTS) from DTE
D	106	Clear to send (CTS) to DTE
E	107	Data set ready (DSR) to DTE
F	109	Received line signal detector (DCD) to DTE
H	n/a	Data terminal ready (DTR) from DTE*
J	n/a	Ring indicator (RI)*
L	n/a	Local loopback (LL) from DTE*
N	n/a	Remote loopback (RL) from loopback
R	104	Received data (RD-A) to DTE
T	104	Received data (RD-B) to DTE
V	115	RX clock (RC-A) to DTE
X	115	RX clock (RC-B) to DTE
P	103	Transmitted data (TD-A) from DTE
S	103	Transmitted data (TD-B) from DTE
Y	114	TX clock (TC-A) to DTE
AA	114	TX clock (TC-B) to DTE
U	113	External TX clock (ETC-A) from DTE
W	113	External TX clock (ETC-B) from DTE
NN	n/a	Test mode (TM) to DTE

\* Ignored by Dual Nx 56/64 Module